OFDM Modulation Using Verilog

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Abstract : In order to improve the transmission velocity in multipath fading wireless channel, the high speed OFDM technology receives increasing attentions in mobile communication. The growth of mobile communications and wireless Internet access has produced a strong demand for advanced wireless techniques. The challenges for wireless communication designs come from the detrimental characteristics of wireless environments, such as multipath fading, Doppler effect, co-channel interference, and intentional jamming in military communications. In this OFDM base band modulation consists of from scrambler, encoder, Serial to Parallel converter, interleaver and Sub carrier modulation (mapping). Sub carrier modulation mostly uses three modes that are BPSK (Binary phase shift keying), QPSK (QuadriPhase Shift Keying) and QAM QAM-4, QAM-6. Interleaver is to disperse lost information to decrease error bit rate, in other words, when user information bits are lost among transmission process. Experimental results indicate that setup time corresponding to transmission velocity and steady time is approximately doubled as setup time, that is, not only achieving the high speed transmission, but also supplying adequate modulation time.

I. Introduction

OFDM requires very accurate frequency synchronization between the receiver and the transmitter; with frequency deviation the sub-carriers will no longer be orthogonal, causing inter-carrier Orthogonal frequency-division multiplexing (OFDM) is a method of encoding digital data on multiple carrier frequencies. OFDM has developed into a popular scheme for wideband digital communication, whether wireless or over copper wires, used in applications such as digital television and audio broadcasting, DSL broadband internet access, wireless networks, and 4G mobile communications. interference (ICI) (i.e., cross-talk between the sub-carriers). Frequency offsets are typically caused by mismatched transmitter and receiver oscillators, or by Doppler shift due to movement. While Doppler shift alone may be compensated for by the receiver, the situation is worsened when combined with multipath, as reflections will appear at various frequency offsets, which is much harder to correct. This effect typically worsens as speed increases, and is an important factor limiting the use of OFDM in high-speed vehicles. Several techniques for ICI suppression are suggested, but they may increase the receiver complexity.

The growth of mobile communications and wireless internet access has produced a strong demand for advanced Wireless techniques. The challenges for wireless communication designs come from the detrimental Characteristics of wireless environments, such as multipath fading, Doppler Effect, co-channel interference, and intentional jamming in military communications. The objective of this paper is to provide an approach to solve the problem of transmission velocity of multipath fading by means of orthogonal frequency division multiplexing. OFDM is a special form of multicarrier modulation, which was originally used in high frequency military radio. An efficient way to implement OFDM by means of a discrete Fourier transform (DFT) was found by Weinstein in 1971. The computational complexity could be further reduced by a fast Fourier transform (FFT). However, OFDM was not popular at that time because the implementation of large-size FFTs was still too expensive. Recent advances in VLSI technologies have enabled cheap and fast implementation of FFTs and IFFTs. In the 1980s, Cimini first investigated the use of OFDM for mobile communications. Since then, OFDM has become popular. In the 1990s, OFDM was adopted in the standards of digital audio broadcasting (DAB), digital video broadcasting (DVB), asymmetric digital subscriber line (ADSL), and IEEE802.11a. OFDM is alsoconsidered in the new fixed broadband wireless access system specification.

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II. Verilog Implementation

Verilog is language that describes electron circuitry and systemic behaves. Based on the description and interrelated software tools, one can gain anticipant circuitry or system. In the article, ISE9.2i achieves various operations of SPARTAN 3 FPGA such as program, synthesis, implement, restriction and simulation

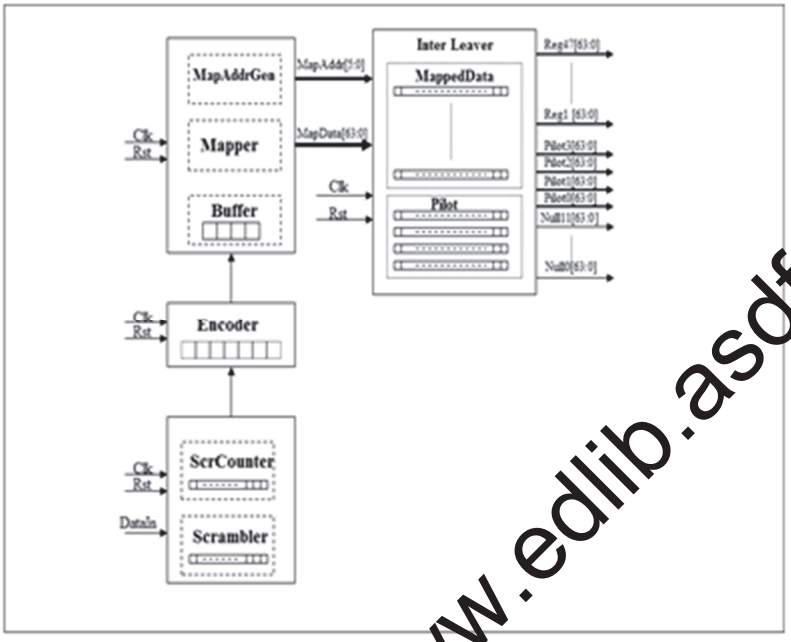

Figure: Block Diagram of OFDM 64 –bit data processor.

In this project we are using QAM-64 modulation technique for implementation of the OFDM data processor. Quadrature amplitude modulation (QAM) is both an analog and a digital modulation scheme. It conveys two analog message signals, or two digital bit streams, by changing (modulating) the amplitudes of two carrier waves, using the amplitude-shift keying (ASK) digital modulation scheme or amplitude modulation (AM) analog modulation scheme. The two carrier waves, usually sinusoids, are out of phase with each other by 90° and are thus called quadrature carriers or quadrature components hence the name of the scheme. The modulated waves are summed, and the resulting waveform is a combination of both phase-shift keying (PSK) and amplitude-shift keying (ASK), or (in the analog case) of phase modulation (PM) and amplitude modulation. In the digital QAM case, a finite number of at least two phases and at least two amplitudes are used. PSK modulators are often designed using the QAM principle, but are not considered as QAM since the amplitude of the modulated carrier signal is constant. QAM is used extensively as a modulation scheme for digital telecommunication systems. Spectral efficiencies of 6 bits/s/Hz can be achieved with QAM. It is being used in optical fiber systems as bit rates increase QAM16 and QAM64 can be optically emulated with a 3-path interferometer.

This research presents an FPGA technique to gain approach in the problem of OFDM system implementation. The proposed design is synthesized by using high-level design tools .The design flow is optimized for fast prototype, which is implemented on the latest generation of FPGA chips. Such an FPGA implementation has the added advantage to modify for changes and improved system performance. The total needed area for the transmitter is taken into account. The total power of OFDM system is 105mw. The proposed design is suitable for low power portable wireless communication in order to obtain long battery life.

The overall System Architecture will be designed using HDL language and simulation, synthesis and implementation (Translation, Mapping, Placing and Routing) will be done using various FPGA based EDA

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Tools(). Finally the proposed system architecture performance (speed, area, power and throughput) will be compared with already existing system implementations.

A. Scrambler

Scrambler is used to randomize the given data i.e; reduce the error rate from the given data. The internal circuit of scrambler consists of LFSR (linear feedback shift register) and a counter. LFSR generates CRC code for error reduction, and the counter is used for counting purpose here we used is a 3 bit counter.

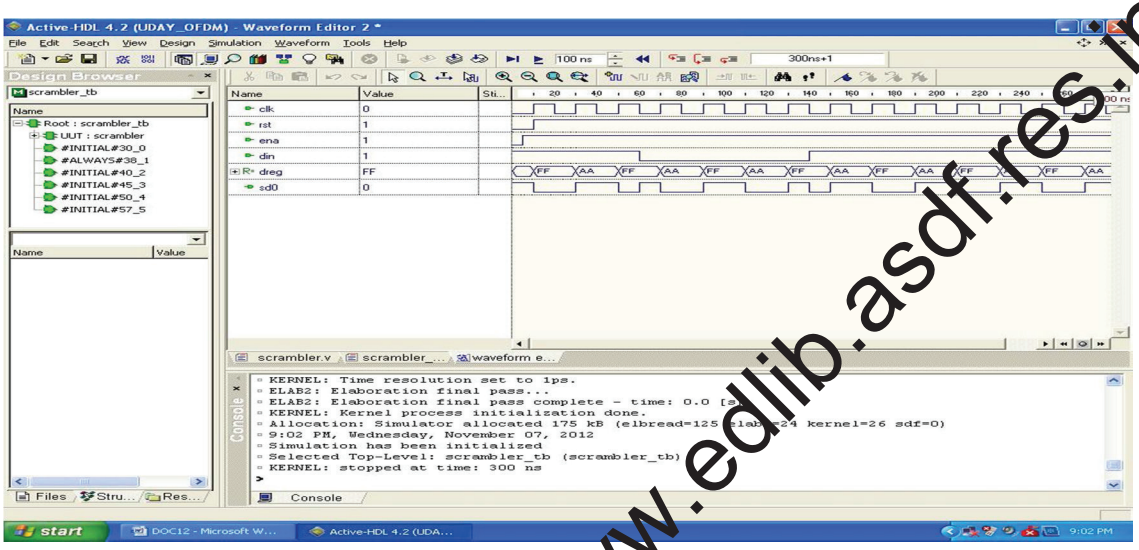

Figure: Simulation results for Time sequence of scrambler.

B. Encoder

We are using convolution encoder for modulation purpose. The main difference between the encoder and lock used here stores the 64 bit data which is comingconvolution encoder is that, for the convolution encoder we are giving 1 bit input then it produces matrix form of output. An internal block of the convolution encoder is shift registers. If rst=0 every rising edge of the clock internal registers are loaded by input bit, then we perform the XOR operation. At the output we get 2 bits of data.

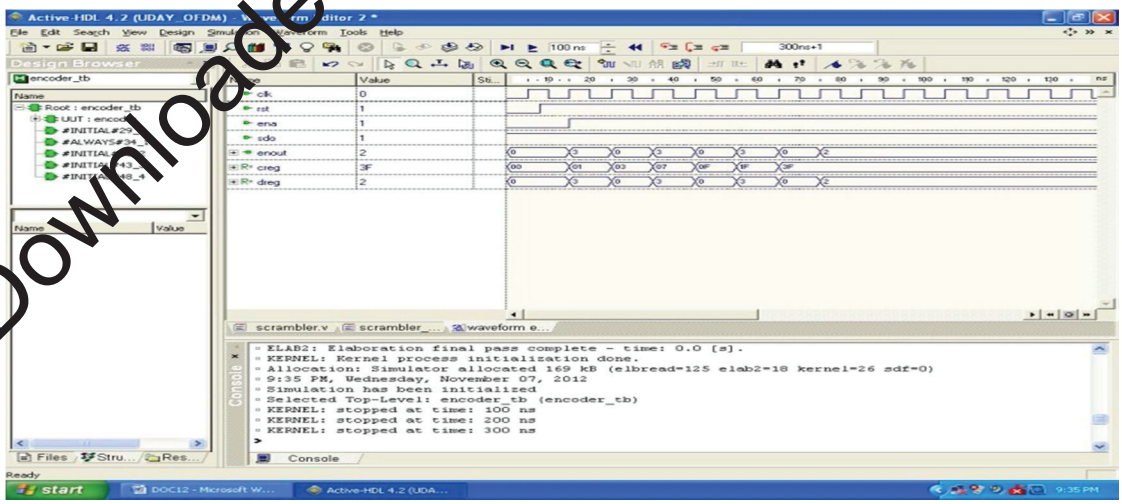

Figure: Simulation results for Time sequence of Encoder.

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C. Mapper

Mapper is used to generate the address for data.it maps useful data and remaining data will be kept a side. Here we are using QAM 6 bit modulation technique. finally we get mapped data and mapped address. When rst=0 then for every rising edge of the clock, 2bits of data is converted into 64 bit data by the mapper and it also generates address for the 64 bits.

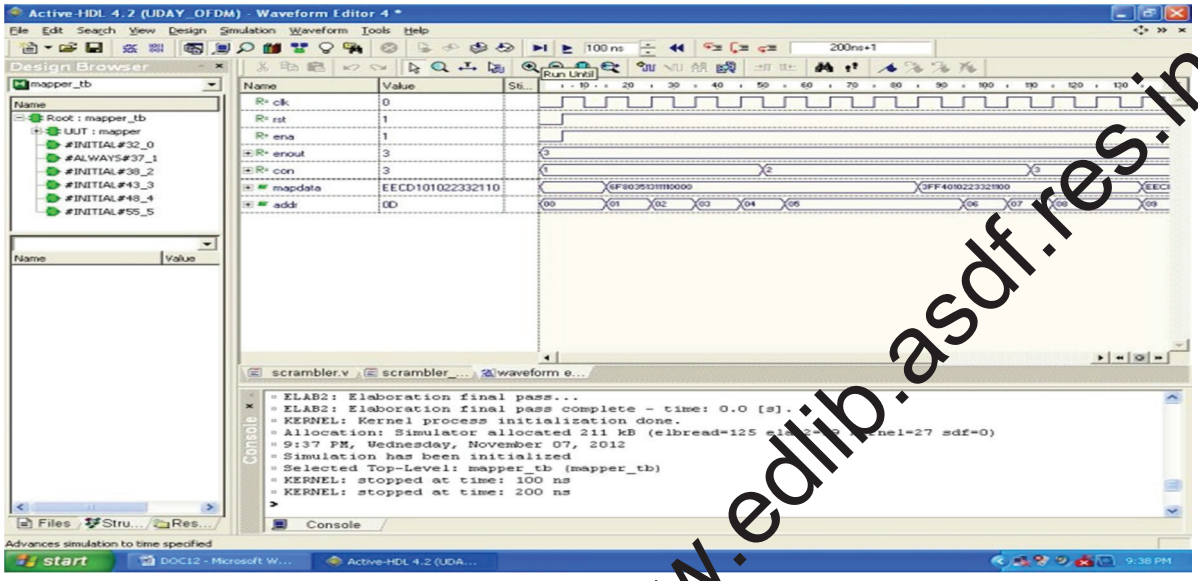

Fig 5: Simulation results for Time sequence of mapper.

D. Interleaver

Register block is also called as Interleaver. It acts as a memory storage device. Register b from a mapper, by using the 64 registers present in it stores the 64bit data and corresponding address of the data.

When rst=0, then for every rising edge of the clock the data from the mapper is loaded into this register block. Finally we get 64 bit data.

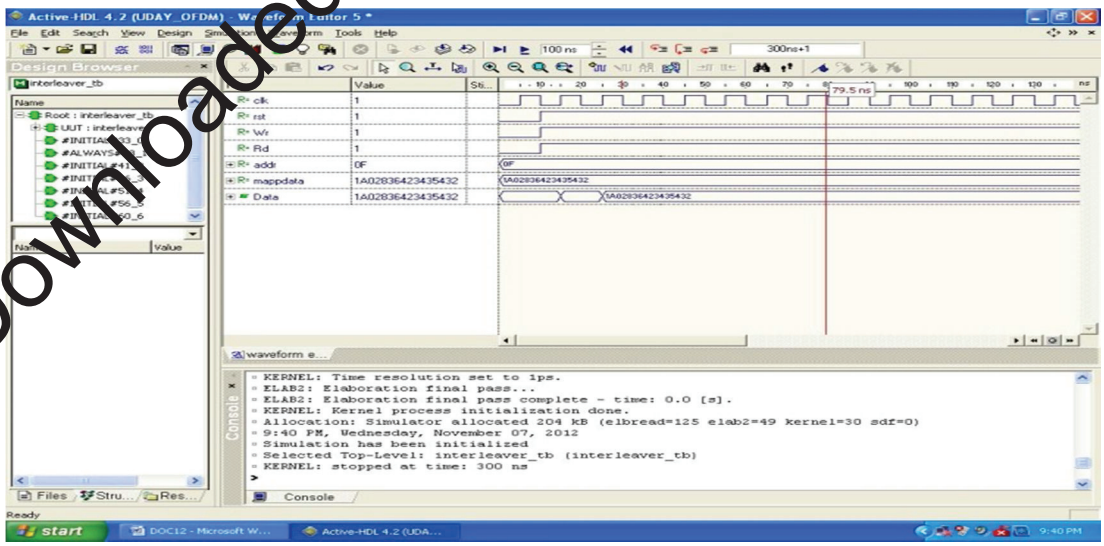

Fig 6: Simulation results for Time sequence of interleaver.

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VI. Conclusion

In this paper, This Paper presents an FPGA technique to gain approach in the problem of OFDM system implementation. The proposed design is synthesized by using high-level design tools .The design flow is optimized for fast prototype, which is implemented on the latest generation of FPGA chips. Such an FPGA implementation has the added advantage to modify for changes and improved system performance. The total needed area for both the transmitter and the receiver is taken into account. The total power of OFDM system is 105mw. The proposed design is suitable for low power portable wireless communication in order to obtain long battery life.

OFDM has various advantages over the previous generation's access techniques. In OFDM, interference's within the cell are averaged by using allocation with cyclic permutations. OFDM enables orthogonality in the uplink by synchronizing users in time and frequency, multi path mitigation without using Equalizers and training sequences, enables Single Frequency Network coverage, where coverage problem exists and gives excellent coverage, spatial diversity by using antenna diversity at the Base Station and possible at the Subscriber Unit.

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