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Digital Multiplier to Multiply Special Integers using ancient Vedic Mathematics

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Abstract- *Multiplier is the basic key of most of the high performance and complex systems like Digital Signal Processors, Microprocessors, and Filters etc. Multiplier design using ancient Vedic mathematics is recent trends of the designers. Recently proposed digital multiplier using the popular sutra "Ekanyunena Purvena" of Vedic mathematics has been analysed in this paper in details. This article clearly demonstrates the detailed architectural diagram, and simulation report of the digital multiplier. The proposed design has been compared with others multipliers and better one has been proposed.*

Keywords: Digital Multiplier, Vedic Mathematics, Ekanyunena Purvena

I INTRODUCTION

The key hardware blocks of almost every high performance systems like digital signal processor, FIR filters, and microprocessors is a multiplier. System performance is greatly influenced by the efficiency of its multiplier. The high speed, simple multiplier design using ancient Vedic mathematics is a recent trend in engineering. The ancient Vedic mathematics has been imported from four Vedas. The word 'Vedic' comes from them other word 'Veda', means collections of knowledge. Jagadguru Shankaracharya Bharati Krsna Teerthaji Maharaja(1884-1960) reconstructed Vedic mathematics from Vedas [1]. It is based on sixteen formulae (sutras). One of the popular sutra in Vedic mathematics is "Ekanyunena Purvena". The recently proposed digital multiplier [2] using Vedic mathematics is the experimental object in this paper. It is a great competitor of popular existing multipliers[3]-[11] like Array multiplier [4], Urdhava multiplier [5], and ROM based multiplier [6]. The detailed architectural design, simulation report, comparison with exiting work, and future scopes of newly proposed digital multiplier [2]are successfully presented in this article. This paper has been arranged as follows. Section II introduces Vedic mathematics, whereas next section discusses about existing works and clearly mentioned about recently proposed digital multiplier [2]. Section IV gives the detailed architectural design of proposed work. The simulation report is attached in section V. Section VI compares the proposed work with existing works. Section VII concludes the work and discusses about future scope.

II VEDIC MATHEMATICS

Vedic mathematics is the part of 'Sthapatya-veda' which is also part of four 'Vedas'. The 'Sthapatya-veda' is an Upa-Veda (supplement) of 'Atharva-veda'. The Vedic mathematics was reconstructed by Shankaracharya BharatiKrishna Teerthaji Maharaja (1884-1960) [1]. After continuous research and development in 'Atharva-veda',swamiji developed 16 formulae and 13 sub-formulae also termed as Sutras and Upa-sutras respectively. The main plat form of ancient mathematical system is nothing but the 16 Vedic formulae, which shows the simple and logical ways of solving problem. The natural ways and the simplicity of solving any type mathematical problems of each mathematical domain increase the acceptance and beauty of Vedic mathematics. Among the all sutras, "Ekanyunena Purvena",

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is very famous. This sutra says the procedure of multiplications as 'One less than the previous' or 'One less than the one before'. This sutra is nothing but a remark of "Nikhilam Navatashcaramam Dashatah". This sutra is used to multiply one integer by 9 or array of 9. The procedure of multiplication using "Ekanyunena Purvena" is discussed step by step below:

a. Left hand side digit is multiplicand. Deduct 1 from the left hand side digit or deduct 1 from multiplicand. It produces present left hand side digit.
b. The right hand side digit is multiplier. Make the difference between the multiplier and present left hand side digit.
c. Just write the two numbers side by side.

Let us discuss with some examples.

Example 1: 5x 9
L.H.S=5(Multiplicand) & R. H. S. = 9(Multiplier)
Step (a) gives 5 – 1 =4 (Present L.H.S. Digit)
Step (b) gives 9 – 4 = 5(Present R.H.S. Digit)
Step (c) The answer is: 45

Example 2: 11 x 99
L.H.S=11(Multiplicand) & R. H. S. = 99(Multiplier)
Step (a) gives 11 – 1 = 10(Present L.H.S. Digit)
Step (b) gives 99 – 10 = 89 (Present R.H.S. Digit)
Step (c) The answer is: 1089

Example 3: 125 x 999
L.H.S=125(Multiplicand) & R. H. S. = 999(Multiplier)
Step (a) gives 125 – 1 = 124 (Present L.H.S. Digit)
Step (b) gives 999 – 124 = 875 (Present R.H.S. Digit)
Step (c) The answer is: 124875

III EXISTING WORK

There are many conventional design techniques of multiplier like array multiplier [4], Urtharba multiplier[5], ROM based multiplier [6] etc., but the newly proposed design techniques is novel. This paper elaborated the design idea of recently proposed Vedic multiplier [2]. This is very helpful for multiplication where the multiplicand is any integer and multiplier is 9 or array of 9 (as for example 99,999,999 etc.). Simple algorithm, flow chart, core architecture, mathematical expression etc. already exists for newly proposed multiplier.

IV PROPOSED WORK

Newly proposed digital multiplier [2] concept has been elaborated in this paper. The detailed architecture, simulation report, RTL schematic, Logic schematic, Device utilization summary, comparison with existing multipliers in terms of delay and simplicity with future scopes have been proposed in this article. The detailed architecture for 4 bits digit is shown in Fig. 1, where A is multiplicand and B is multiplier. The leftmost subtractor subtracts '0001' from 'A'. The right most subtractor subtracts the subtractor1's output from 'B'. The results of two multipliers fed into array of resistors as shown in Fig. 1. The resistors save the results and give the output. The proposed multiplier's architecture is tested and verified using the tool 'Xilinx ISE14.2' [12]. The RTL schematic diagram of proposed digital multiplier circuit looks like the Fig. 2. The Expanded RTL schematic of this Vedic multiplier is shown in Fig. 3. The multiplier architecture using block diagram is shown in Fig. 4. The technological schematic of the multiplier in Xilinx ISE14.2 is shown in Fig. 5.

V SIMULATION REPORT

The proposed multiplier has been tested and verified in Xilinx ISE14.2 software tool. The snap shot for multiplicand and multiplier, with result shown in Fig. 6; hence it indicates that the multiplier has been run successfully. Fig. 7 shows the details project status report of the multiplier during the simulation.

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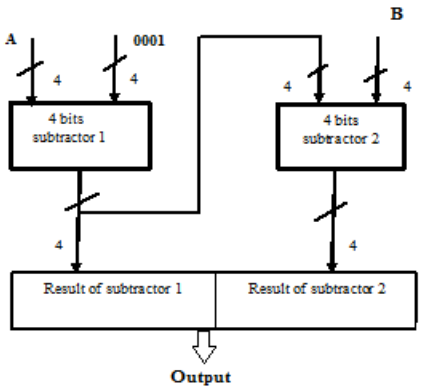

Figure 1. Architecture of multiplier for 4 bits

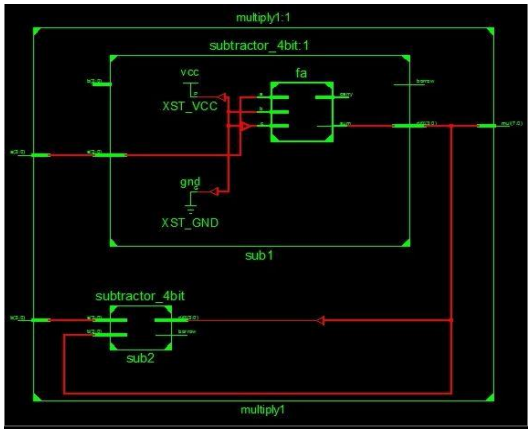

Figure 2. RTL schematic diagram of proposed multiplier

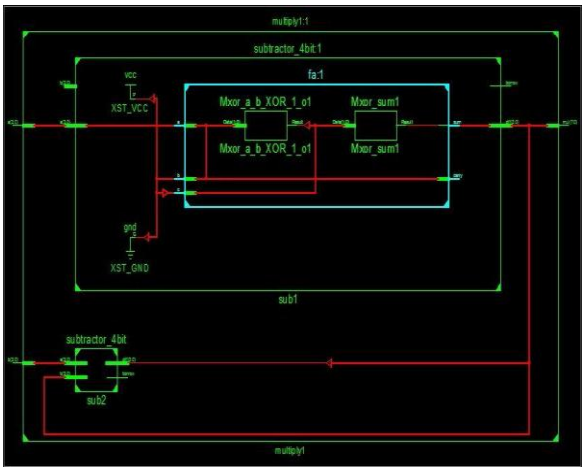

Figure 3.Expanded RTL schematic of multiplier

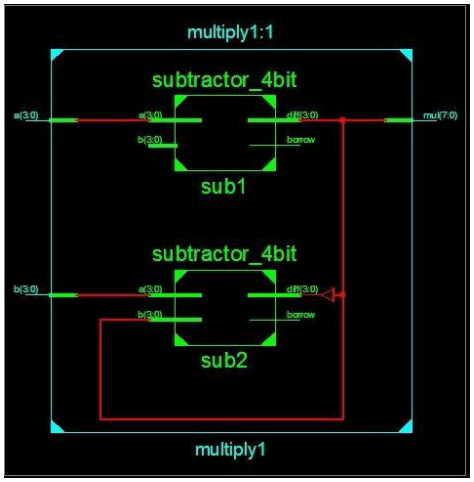

Figure 4. Block diagram of proposed multiplier

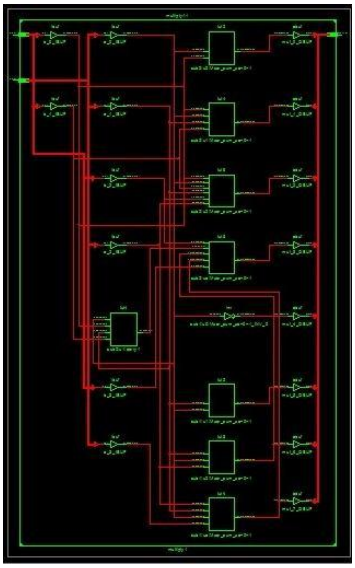

Figure 5. Technological Schematic diagram

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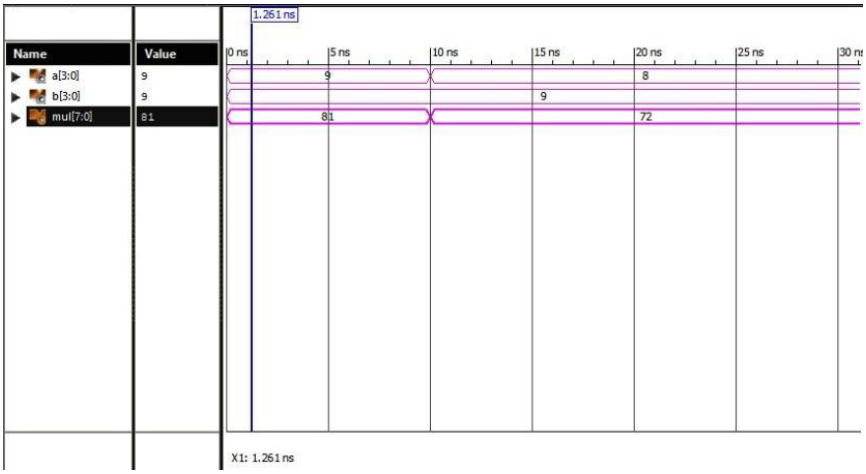

Figure 6. Simulation report

Multiplier 4bit Project Status (02/02/2015 - 23:03:15)			
Project File:	multiplier1.xise	**Parser Errors:**	No Errors
Module Name:	subtractor_4bit	**Implementation State:**	Translated
Target Device:	xc6vcx75t-2ff484	• **Errors:**	No Errors
Product Version:	ISE 14.2	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Figure 7. Project status report of proposed multiplier

VI COMPARISON WITH EXISTING WORK

The design approach of Vedic multiplier using the sutra "Ekanyunena Purvena" has been done successfully in this paper. The architecture of multiplier design has been simulated nicely. Simulation result has been seen and the calculated delay from the simulation result has been compared to other existing techniques. The device utilization summary and comparative delay study of different multipliers with respect to proposed multiplier has been shown in Fig. 8 and Fig. 9 respectively.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	6	46560	0%
Number of fully used LUT-FF pairs	0	6	0%
Number of bonded IOBs	13	240	5%

Figure 8. Device utilization summary

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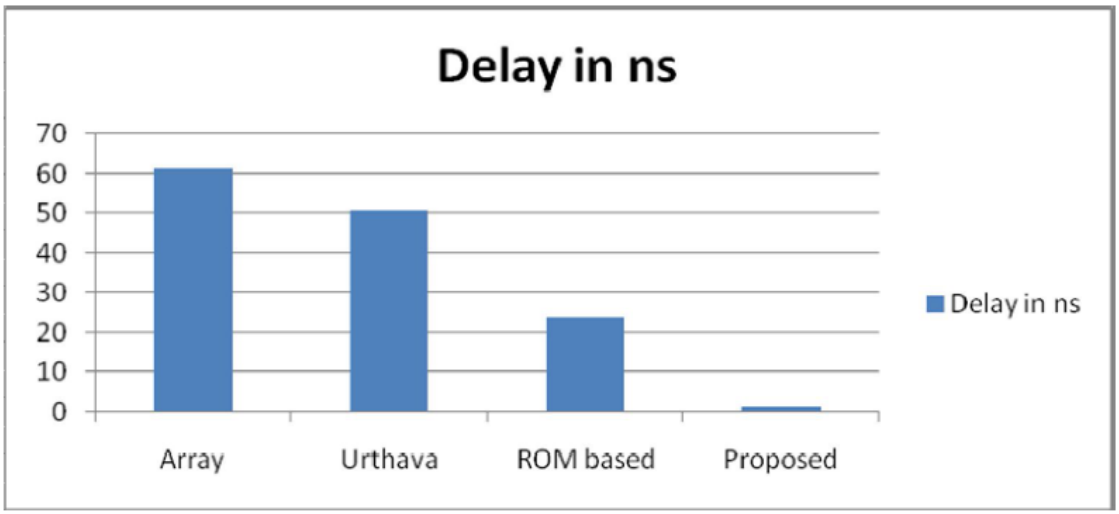

Figure 9. Bar graph of delays of different multiplier

VII CONCLUSION AND FUTURE SCOPE

In this paper the approach has been simulated using the popular tool Xilinx ISE14.2 and the speed &performance of the circuit has been tested as well. This design indicates a high efficient design approach of Vedic multiplier. The computational path delay for 4×4 bit Vedic digital multiplier is 1.605 ns. It is observed that this multiplier is much more simple and efficient than others multiplier. The natural and quick method of Vedic multiplication makes this method easier. The simplicity & novelty of this work differentiate it from the other approaches. The hardware implementation is necessary for real time application. In future the approach may be used in the other sutras or sub sutras of Vedic mathematics to design the quick multiplier. The digital design may be transferred to VLSI technology for better performance.

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