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An effective clock generator for Heterogeneous GALS in CMOS technology

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Abstract: *It is so complicate to present clock generator for GALS (Globally Asynchronous Locally Synchronous) MPSoCs (Multiprocessor Systems-on-chip) and here we are going to produce ADPLL (All-Digital Phase-Locked Loop) clock generator that consumes very low power of 2.7 mW and it has very small chip area of 0.0078 mm. These ADPLL clock generators are used in fine-grained power management such as DVFS per core and it contains phase rotation and frequency division blocks which are used to generate multiphase clock signal since that frequencies of core varies from 83 to 666 MHz with 50% duty cycle. Such clock should encounter the stipulation of DDR2/DDR3 memory interfaces and in addition it renders a devoted eminent-speed clock up to 4 GHz for serial data links of network-on-chip. And, in fast dynamic frequency scaling applications the core frequencies varies randomly in one clock cycle. Finally, a prototype in 65-nm CMOS technology varies the performance of statistical analysis of mismatch.*

Keywords: All-digital Phase-Locked Loop (ADPLL), Digitally Controlled Oscillator (DCO), Dynamic Voltage and Frequency Scaling (DVFS), Globally Asynchronous Locally Synchronous (GALS), Multiprocessor Systems- on-Chip (MPSoCs).

I.INTRODUCTION

MPSoCs (Multiprocessor systems-on-chip) render compromising solutions for baseband operations which support a broad range of radio standards are supported and eminent energy efficiency is compulsory for mobile terminals. [1]. In order to encounter such requirements, the heterogeneous MPSoCs let in dissimilar cores such as general purpose RISC processors, DSPs (digital signal processors), or hardware accelerator and in addition on-chip data transmission structures as though NoC (Network-on-Chip) eminent-speed links and I/O components such as DDR (double-data-rate) [2] memory interfaces or FPGA (Field-Programmable Gate Array) associations are division of complex MPSoCs and they possess differentiated necessitates for clock frequency and clock quality like jitter and duty cycle respectively. [3,4].

Usually, concentrated clock generators are employed that render clocks for multiple cores and I/O interfaces in heterogeneous Multiprocessor systems-on-chip and the 80 core processor [5] employs meso-synchronous clocking with an individual PLL only that does not permit single per core frequency scaling. In demarcation, GALS (Globally Asynchronous Locally Synchronous) clocking architectures render each and every core with a devoted clock deflecting global eminent-speed synchronous clock dispersion networks [6]. In order to provide further increase in energy efficiency, fine grained power management method like dynamic voltage and frequency scaling (DVFS) are necessitated[7], [8].

The independent local clocks are present in GALS MPSoCs in which per-core DVFS can be effectively implemented. Results for

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extremist-fast provide voltage variations have been described [7]. Hence, a quick reacting clock generator is needed to recognize such fast DVFS approaches that minimize core idle times while varying the level of performance and enhance entire throughput of the system. [9] and [10] necessitates wide-eyed ring oscillators for Globally Asynchronous Locally Synchronous cores, that however are not desirable for DVFS. [11] employs locally graduated clock generators that are based on the controlled delay lines, but it does not have fast core frequency switching.

[8] employs an assembled ring oscillator for quick DVFS that cannot produce modest jitter clocks at determined frequencies because they are not locked to a mentioned clock. [12] proposed various clock generators that are based on flying adder (FA) frequency synthesis, that can produce a broad range of frequencies with modest jitter, but it necessitates prominent chip area. Believing the style for integration of several-core MPSoCs [5], compromising clocking solutions are needed to fulfill the requirements of clock quality and endure progressed fine-grained power management approaches. Thus, such operation provides a modest chip area, reduced power ADPLL (All-Digital Phase-Locked Loop)-based clock generator for per-core representation in heterogeneous GALS MPSoCs, rendering both a broad range of output frequencies and differentiated eminent-speed clocks. It modifies hyper-fast frequency switching for per-core DVFS systems.

II. ALL-DIGITAL PHASE-LOCKED LOOP (ADPLL)

The ADPLL of Fig. 1 has a structure and operation very similar to a second-order CPPLL. The principal difference is that the phase error information is processed in different domains. In the all-digital PLL, the UP and DN pulses are overlapped, and the result is digitized and processed by a digital filter. For the CPPLL, a charge pump (CP) is used to generate a charge which is proportional to the time difference between the UP and DN pulses. The resulting charge is pumped into the analog filter, the output voltage of which controls the VCO. This similarity allows one to extend the design procedure for a second-order CPPLL to a second-order ADPLL.

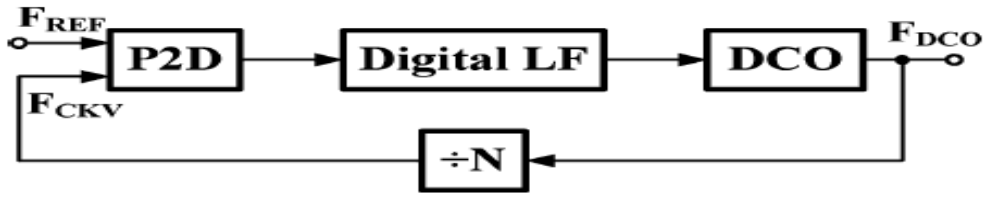

Figure 1: All Digital PLL

III. DYNAMIC VOLTAGE AND FREQUENCY SCALING

DVFS (Dynamic voltage and frequency scaling) is a generally employed proficiency to preserve power on a broad range of calculating systems such as embedded systems, laptop, desktop systems and eminent-performance server-category systems. DVFS can be able to minimize the consumption of power of CMOS integrated circuit, like a modern computing processor, by minimizing the frequency at that it works is shown by,

$$W = C_p f v^2 + P_{stat}$$

Where C_p is the transistor gate capacitance that reckons on boast size, f is the working frequency and v is the supplied voltage and the voltage necessitated for static operation is decided by the frequency of the circuit which is clocked. These can be minimized if the frequency is also minimized and this can be affording a substantial reduction in consumption of power since it has the v^2 relationship which is shown in above equation.

IV. GLOBALLY ASYNCHRONOUS LOCALLY SYNCHRONOUS

GALS (Globally Asynchronous Locally Synchronous) Systems merge the gains of systems such as synchronous and asynchronous systems and the modules are planned like modules in a globally synchronous plan, employing the similar tools and methodologies. Each and every block is severally clocked that assists to relieve clock skew and links among the synchronous blocks may be asynchronous. When data moves into a synchronous system from an asynchronous system, registers in that input are prostrate to metastability. In order to obviate this, the reaching of data is suggested by AHP (Asynchronous Handshaking Protocol). When the data reaches, the topically generated clock is hesitated: in exercise the arising edge of that clock is detained.

Once data is securely arrived, the clock is relinquished so data is connected with zero probability of the metastability on the path of data. [14] utilized ME components to intercede between the clock and the entering requests that assisted to excrete metastability. [15] presented wrappers of asynchronous systems, ideal components that can be located throughout synchronous modules to render the handshake signals and build them GALS modules and the local clock generator is fabricated from inverter and a delay line which is alike with an inverter ring oscillator. The trouble of utilizing such inverters is that which alone has a delay line and it is very difficult to exactly tune the clock period as operation variations and temperature impress the delay. Thus exact delay lines are formulated that can be able to maintain a static clock frequency [16], [17].

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V. MULTIPROCESSOR SYSTEMS-ON-CHIP

MPSoCs (Multiprocessor systems-on-chips) have issued in past few decades as a significant class of VLSI (Very Large Scale Integration) systems and the MPSoC is a system on-chip, a VLSI system which integrates most of the components essential for an application and which utilizes MPP (Multiple Programmable Processors) as their system components. Multiprocessor systems-on-chips are widely employed in networking, communication systems, digital signal processing, multimedia and other applications.
MPSoCs substantiate as an essential and discrete branch of multiprocessors and they are not merely conventional multiprocessors reduced to a single chip but are planned to fulfill the unequalled necessities of embedded features. MPSoCs have been in production for much longer than multicore processors. We argue in this section that MPSoCs form two important and distinct branches in the taxonomy of multiprocessors: homogeneous and heterogeneous multiprocessors. The importance and historical independence of these lines of multiprocessor development are not always appreciated in the microprocessor community.

VI. DIGITALLY CONTROLLED OSCILLATOR

Phase-Locked loops (PLLs) are widely used in many communication systems to clock and data recovery or frequency synthesis. Traditional analog circuit design such as PLL shifts the design paradigm toward more digitally intensive techniques, easier testability and less parameter variability because of process migration. A digitally controlled oscillator (DCO) based architecture for RF frequency synthesizer was reported in [1]. The LC tank DCO achieves very fine frequency resolution (23 kHz) by using advanced 0.13- m CMOS process. The switchable capacitance of the finest pMOS varactor is 38 attofarads. However, this DCO suffers from one fundamental drawback. Due to the extremely small size of varactor, it requires intensive circuit layout and needs advanced lithography technology. A long design cycle will occur as product design transfers to different processes or the design specifications are changed. Thus, this work attempts to propose a high resolution DCO by using NOR/NAND gates as novel varactor.

VII. EXPERIMENTAL RESULTS

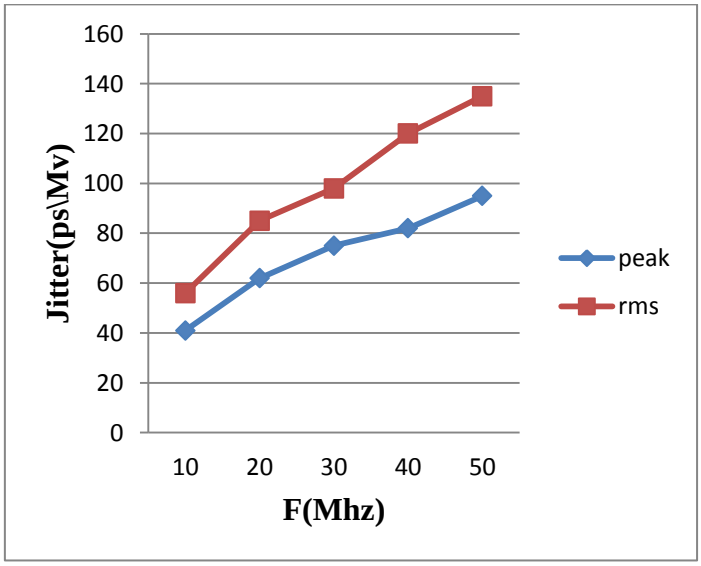

Fig 1:Performance Compared between Peak and Rms value according to Frequency and Jitter

VIII. CONCLUSION

Thus, we presented ADPLL (All-Digital Phase-Locked Loop) clock generator with low power consumption and very small chip area and such ADPLL contains DCO which only has analog custom components that guide to ultra small die area and in modern technologies these ultra small die area can scale well. The feature of DCO is to provide a new power-down strategy to assure save start-up and the open loop schemes are used to generate output clocks that permits instant variations in frequencies with no time-consuming ADPLL re-lock which renders fast frequency scaling in fine grained DVFS architectures. Moreover, such clock generators are renders a broad range of frequencies from 83MHz up to 4 GHz for core clocking, special purpose DDR2/3 clocks and high-speed NoC clocks. The performance is evaluated by test chip measurements in TSMC 65-nm LP CMOS technology and statistical measures demonstrate the robustness with respect to mismatch variations. Such phase mismatch effects in phase rotating frequency dividers is not an important effect for the directed application. The capacity of operation in MPSoC environments have been tested by noise sensitivity tests. Hence, our proposed circuit renders an effective new clocking solution for low-power consuming heterogeneous MPSoCs.

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