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A Level-up Shifter using MTCMOS Technique for Power Minimization

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Abstract- Level shifter is an interfacing circuit which can interface low core voltage to high input-output voltage. It allows communication between different modules without adding up any extra supply pin. The main objective of the work is to minimize power dissipation in shifter circuit, which is due to different supply voltages in the circuit. The proposed method uses MTCMOS technique, which is one of the low power design technique to achieve power minimization. The new circuit uses the multi-threshold CMOS technique to provide a wide voltage conversion . The proposed design is implemented in CADENCE Virtuoso 180-nm CMOS technology. The new LS reaches a propagation delay value of 17 ns, a static power dissipation of only 115.3 pW, for a 1-MHz input pulse.

Keywords- Level Shifter, Sub-threshold, MTCMOS, low power, low voltage.

I. INTRODUCTION

The most direct way to reduce power dissipation in digital LSIs is to reduce supply voltage. Several low power design techniques were used. Sub-threshold LSI is the most widely used in power aware applications. However there are a number of design challenges imposed and several studies were carried out. Among the techniques known in the literature to reduce power consumption, those based on power supply voltage reduction are considered very effective even though they can severely penalize speed performances . An alternative approach, known as the multi-supply voltage domain technique , consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements.
A key challenge in the design of efficient multiple-supply circuits is minimizing the cost of the level conversion between different voltage domains while maintaining the overall robustness of the design. To such a purpose, level shifter (LS) circuits have to be used. Traditionally, level shifter circuits were used to allow chip core signals to be transmitted to the outside world through the pad ring, which often operated with different voltage levels.

II. CONVENTIONAL LEVEL SHIFTER METHOD

The conventional LS (Level Shifter) circuit consists of level conversion circuit and a logic error correction circuit (LECC) [3]. The complementary input signals (IN and INB) and the output signal (OUT) are applied to the LECC. Figure 1 shows the schematic of the conventional level shifter circuit. The operation principles of the circuits are described in the following sections.

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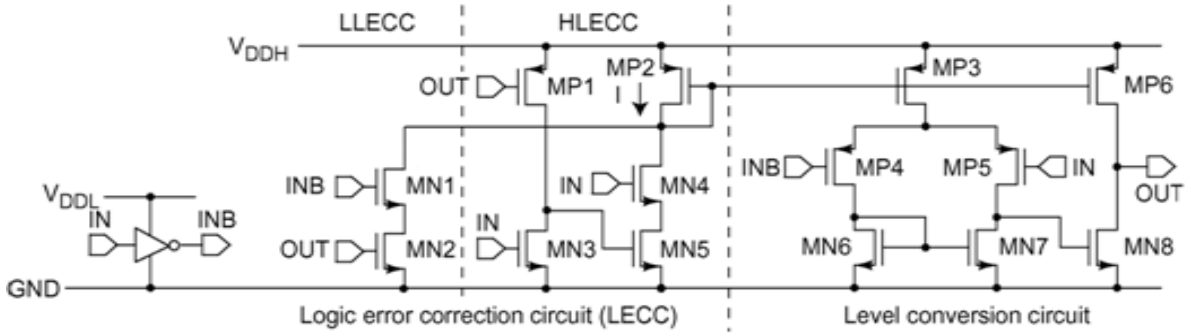

Fig. 1 Schematic of conventional Level Shifter Circuit

The LECC, which is shown on the left in Fig. 1, consists of two circuit blocks:

- a low logic error correction circuit (LLECC) and
- a high logic error correction circuit (HLECC).

The LECC generates an operating current such that IN and OUT correspond to each other. When the output logic level of the LS circuit corresponds to the input logic level, the LECC does not supply current . When they do not correspond, the LECC detects the logic error, and the LLECC or HLECC supplies an operating current. In other words, the LECC supplies an operating current only when the input and output logic levels do not correspond to each other. When IN and OUT correspond, the LECC does not supply any current to the level conversion circuit. However, in fact, leakage current flows in the circuit. However, when the input voltage signal is high, the output node of the current mirror floats, thus negatively impacting the overall power consumption.

The level conversion circuit, is based on a conventional two-stage comparator circuit which generates output voltage signal, OUT, according to the difference in the voltage of IN and INB. The output voltage is determined by the drive currents of pull-up transistor MP6 and pull-down transistor MN8, and the currents flowing in MP6 and MN8 depend on current flowing through MP2.

A. Drawbacks

In this conventional comparator design, a current reference circuit needs to operate steadily. However, because the current reference circuit dissipates static current and increases power dissipation , it proves impractical to use.

III. PROPOSED LEVEL SHIFTER CIRCUIT WITH MTCMOS TECHNIQUE

The circuit diagram of proposed level shifter circuit based on MTCMOS technique is shown in figure 2.

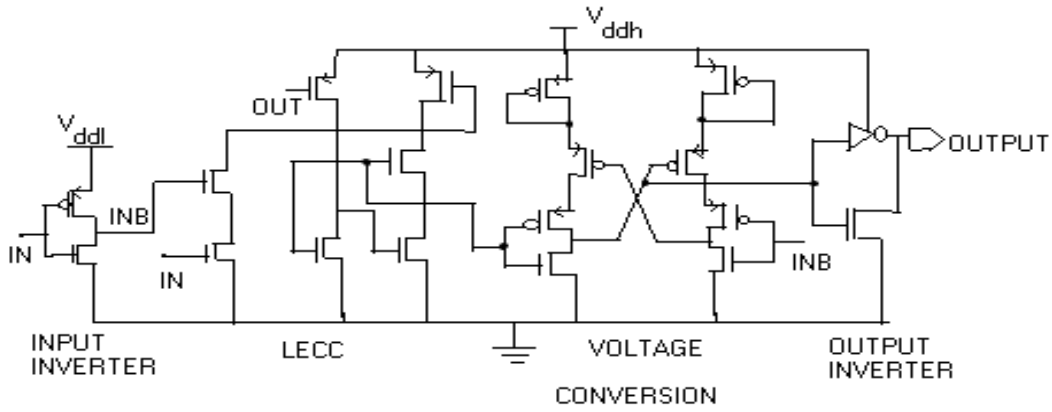

Figure 2. Schematic of Proposed Level Shifter Circuit based on MTCMOS Technique

A. Input Inverter

The input inverter consists of PMOS and NMOS transistors. They are driven by a lower supply voltage VDDL . The source of the PMOS transistor is connected to low supply voltage and the drain of NMOS is connected to ground.

B. LECC (Logic Error Correction Circuit)

The LECC is driven by IN, INB, and OUT. The LECC generates an operating current such that IN and OUT correspond to each other. When the output logic level of the LS circuit corresponds to the input logic level, the LECC does not supply current . When they do not correspond, the LECC detects the logic error.

C. Voltage Conversion Stage

The voltage conversion circuit is based on DCVS (Differential Cascode Voltage Switch) logic. The circuit is designed with low-voltage threshold (lvt), standard voltage threshold (svt), and high-voltage threshold (hvt) transistors. To provide fast differential low-voltage input signals and to increase the strength of the pull-down network of the main voltage conversion stage, the input inverter was created using lvt devices. To reduce the effect of cross bar current flowing in the nodes NH and NL, two lvt PMOS devices are adopted.

D. Output Inverter

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The voltage conversion stage is connected to the output inverter so as to measure the required output of the proposed circuit.

IV. RESULTS

The proposed circuit is implemented in CADENCE – Virtuoso tool and implemented in 180 nm CMOS technology. Figure 3 shows the schematic drawn in Cadence tool. The circuit dissipates 115.3pW of static power with the supply voltage of less then 2V(1.8V). The fig.4 and fig. 5 shows the simulated waveform in Cadence and power spectral graph. Table 1 shows the performance comparison of various level shifter circuits. The table shows a considerable reduction in static power.

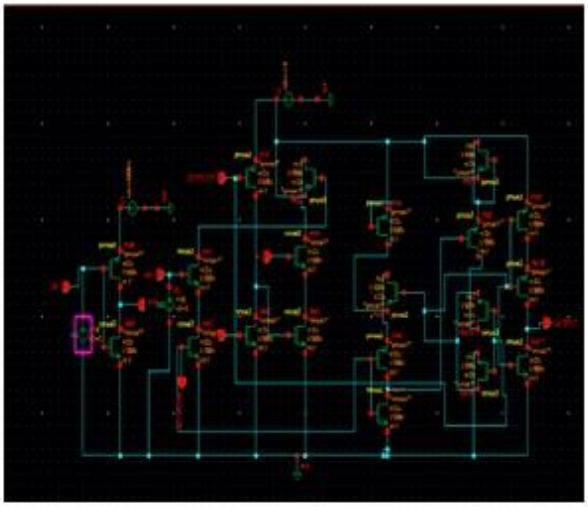

Figure 3. Schematic Circuit drawn in Cadence

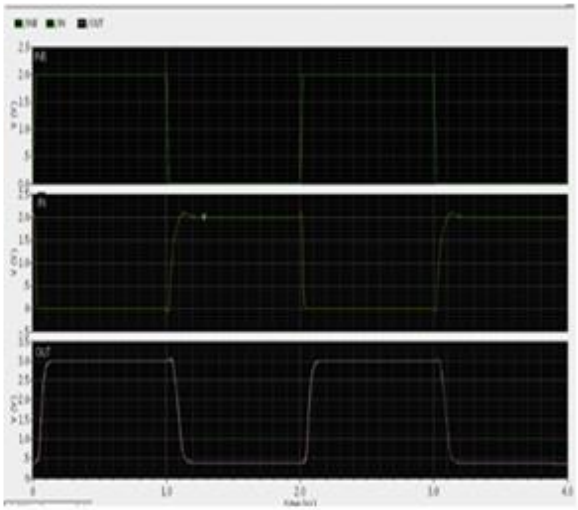

Figure 4. Level Shifted Waveform in Cadence

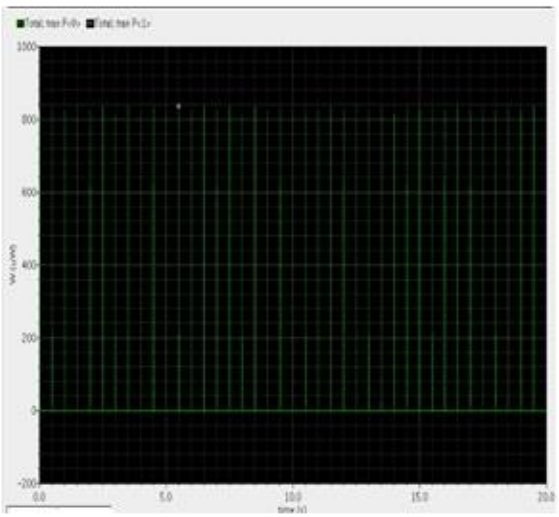

Figure 5. Power Spectral Graph of Proposed Circuit

Parameter	Conventional LS	Proposed LS
Type of technology	350 nm	180 nm
Type	Comparator	DCVS
V_{DD} (V), f_{IN} (Hz)	0.4, 10 kHz	0.23, 1 kHz
V_{DDL} (V)	0.23 V	0.2 V
V_{DDH} (V)	3 V	2.5 V
Static Power (nW)	58 nW	115.3 pW

Table 1. Performance Comparison Table

The power dissipation of the proposed LS circuit can be expressed as

$$P = P_{dyn} + P_{int}$$
$$= C_L V_{DDH}^2 f_{IN} + I_{AVG} V_{DDH} \quad (1)$$

where I_{AVG} is the average current flowing through the circuit.

V. CONCLUSION

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The proposed level shifter circuit with MTCMOS circuit is presented and it is simulated in Cadence Virtuoso tool. The proposed circuit with MTCMOS technique is implemented in 180-nm CMOS technology. The static power dissipation achieved was 115.3 pW with the supply voltage of 0.2 V.

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