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# Implementation of Efficient Analog to Digital Converter using Multi-Input Double-Tail Comparator

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**Abstract-** *Dynamic comparators are widely used to design Analog-to-Digital converters (ADC) due to its high speed and low power consumption. The regenerative delay can be reduced by using double-tail comparators. The delay and power consumption can be further reduced by using improved double-tail comparators. By increasing the number of comparisons per clock cycle the speed can be increased and the total area of the ADC can be reduced effectively. Simulations are carried out in 180-nm CMOS technology.*

**Index Terms-** *Dynamic comparator, Double-tail, Flash ADC, Multi-input.*

## 1. INTRODUCTION

High speed application such as communication system, wireless systems, EEG or ECG controlling unit, touch screen devices requires high speed ADC designs. Flash type ADCs are the fastest, since the digital output can be obtained in a single clock cycle. Comparators are the fundamental component in all ADC design [1]. To increase the speed of ADC high speed low power consuming comparators are widely preferred.

Successive approximation ADC includes comparator, Digital to Analog Converter (DAC) unit and a register. The conversion takes place in a series of clock cycles. Delta-sigma ADC includes an integrator, comparator, counter, summing interval and a buffer. But the accuracy is very less and makes the design less reliable. Many researches are made to increase the speed of the design. One such technique is to design high speed comparators.

Operational amplifiers (Op-amp) were initially used as comparators [1]. The output is high only if the applied input is larger than the other input. The disadvantage of op-amps was its high static power and regenerative delay. Static and Pre amplifier based comparators were developed to increase the speed but the kick-back noise [4] is high and impedance matching problem exists. Optimum solution is obtained by using regenerative comparator design.

## 2. Regenerative Comparators

The comparator design is chosen based on many performance factors such as low power, low kick-back noise, less area, rail-to-rail output swing, offset etc. It is noted that the most commonly used comparator is the dynamic comparator.

### A. Dynamic Comparator

Dynamic comparator is chosen because of no static power consumption [2], [3]. The schematic diagram of comparator is shown in



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Fig.1, the two phases of operation is carried out by setting the clock (CLK) signal. CLK is set to ground in reset phase and Mtail1 is off transistors M7 and M8 are on, which pulls the two output nodes $Out_n$ and $Out_p$ charged to VDD. CLK is set to VDD in the comparison phase turning on $M_{tail}$, discharging the output nodes to ground. The inputs INN is applied to transistor M1 and INP is applied to M2 respectively. The discharging rate depends on the applied input (INN/INP).

Assuming that input INN>INP the discharging rate $Out_p$ is high compared to $Out_n$. In a mean time $Out_p$ completely discharges to ground. The outputs are fed to latch network, consisting of cross-coupled inverters. Discharging of $Out_p$ turns on the corresponding PMOS transistor M5 which charges the $Out_n$ to VDD. Thus VDD at $Out_p$ indicates INN > INP and zero at $Out_p$ indicates INP > INN.

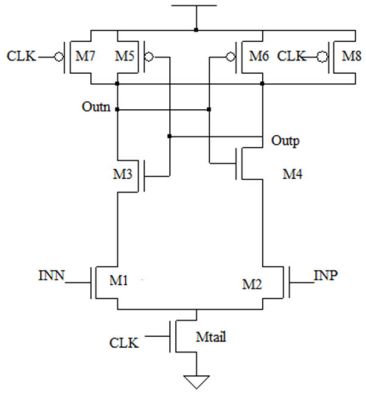


Fig. 1 Conventional dynamic comparator

The delay in comparator is the sum of latch delay and delay due to discharge of load capacitance. On analysis it is seen that by reducing the latch delay the total delay can be decreased. The advantage of dynamic comparator is the rail-to-rail output swing, high input impedance and no static power.

The drawback of the design is increased due to stacking of transistors at the input, which requires a high supply voltage for proper delay. On the other hand by increasing the common mode voltage difference the latch regenerative delay can be reduced.

## B. Conventional Double-Tail DYNAMIC Comparator

A conventional double-tail comparator is designed with less stacking of transistors compared to the previous model. The schematic diagram is shown in Fig.2 where the differential amplifier pair and the latch circuit are separated and Mtail2 p-MOS transistor is added in the latch design [2], [3]. Mtail2 enables high speed latching independent to input common-mode voltage. Two transistors MR1 and MR2 are added to provide shielding of the cross-coupled inverters (latch) and to reduce the kick back noise. Two phases of operation is observed in the conventional double-tail comparator design. In the reset phase CLK is set to zero. It turns off Mtail2 and Mtail1 and transistors M3 and M4 are turned on. The nodes $f_n$ and $f_p$ are charged to VDD and discharges the output to ground, by turning on transistors MR1 and MR2.

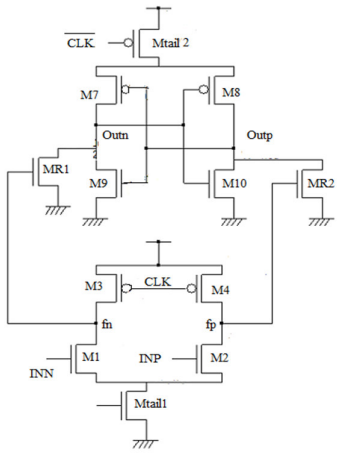


Fig. 2 conventional Double-tail comparator.

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In the decision making phase or comparison phase CLK is set to VDD turning on Mtail2 and Mtail1. Transistors M3 and M4 are turned off, discharging the nodes fn and fp. The discharging rate depends on the differential common mode voltage $\Delta V_{fn}$. Assuming INP>INN, voltage at node fp discharges quicker than node fn turning on latch transistor M9. The corresponding output ($Out_n$) discharges to ground, turning on transistor M8 and charging the other output $Out_p$ to VDD. Thus the two input voltages can be compared by observing the output voltages. Similarly when INN>INP, $Out_n$ is high $Out_p$ is low.

The less stacking of transistors enhances reduced delay and the circuit can be operated at very low supply voltages. Due to charging of transistors MR1 and MR2, power consumption is increased.

## C. Improved Double-Tail Dynamic Comparator

The aim of the design is to reduce the regenerative delay by adding two cross-coupled transistors MC1 and MC2 as shown in Fig. 3. The comparator operations are carried in two phases [3]. In the reset phase CLK is set to zero. Both the $M_{tail}$ transistors are off, M3 and M4 pulls the node fn and fp to VDD. Transistors MR1 and MR2 turns on and pulls the output nodes to ground. Two n-MOS (Msw1 and Msw2) transistors are added near the input transistors to reduce the static power consumption.

In the comparison phase CLK is set to VDD both the tail transistors are on, charging the output nodes. Transistors M3 and M4 are off which decays the voltage at nodes fn and fp. The discharging rate also depends on the applied input voltages.

Consider a case if input INP>INN node fn discharges to ground quicker than node fn, which turns on one of the cross-coupled transistor and pulls the node fp back to VDD. A high voltage at node fp drops the output ($Out_n$) to ground which turns on transistor M8 in latch circuit and charges the output node $Out_p$ to VDD.

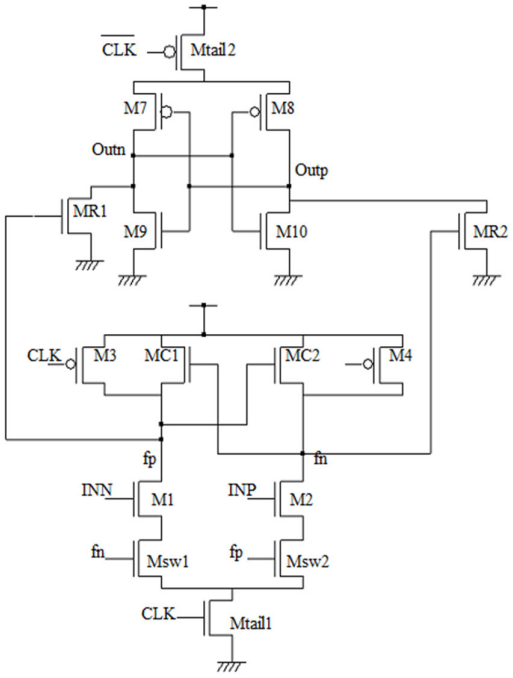


Fig. 3 Improved Double-tail comparator

Thus the two applied voltage can be compared based on the output. Comparing with conventional dynamic comparator, the area of the comparator is increased. Simulated analysis shows that, the static power consumption is reduced and the regenerative delay or the speed of comparison is increased more than 10 times. The latch effective trans conductance is increased due to the intermediate stage transistors, increasing the speed of comparator.

## D. Proposed Multi-Input Double-Tail Comparator

Double-tail comparator is used to compare only two inputs in one clock cycle. If the stages of comparison are increased to N times, then N inputs can be compared within one clock signal. Thus the speed can be increased and area can be reduced effectively.

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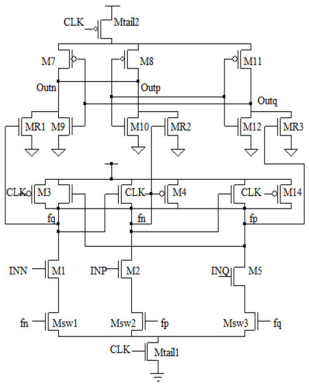



Fig. 4 Multi-input Double-tail Comparator

The operation of a three input comparator is as same as the two input comparator. The schematic is as shown in Fig.4. When CLK is zero all the outputs are zero, nodes fn, fp, fq are high. When CLK is high the inputs INN, INP, INQ are applied. The nodes fn, fp, fq starts discharging.

The rate depends on the applied input also. Consider a case if INN>INP>INQ node fp discharges to zero faster which in turn charges both the other nodes to VDD and corresponding output falls to zero. Zero voltage at node fp causes the output node $Out_n$ to charge to VDD. If INP> INN> INQ output $Out_p$ charges to VDD. If INQ>INN>INP the output $Out_q$ charges to VDD.

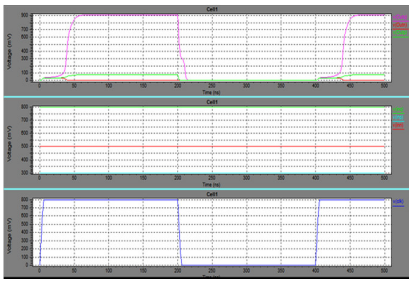
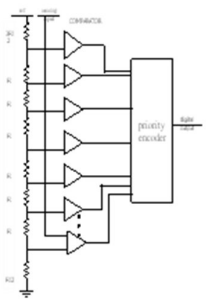


Fig. 5 Output of multi-input comparator.

Thus the three inputs can be compared within a single clock cycle. If the number of stages are increased and applying the above concept more number of inputs can be compared effectively. The simulation is carried out in 180-nm CMOS technology and the output is shown in Fig 5.

## 3. Design of Flash Type Analog to Digital Converter

Comparators are major component in Flash ADC design. In the conventional N-bit Flash ADC, 2N-1 comparators are used. The analog input is applied as one input to the comparator [5], [6]. The reference voltage is applied to resistor ladder. The other input of comparator is obtained from the resistor ladder. To obtain the binary (digital) output, the comparator's outputs are fed to the priority encoder. Consider a 3-bit Flash ADC shown in Fig.6. It consists of 7 comparators and 8 to 3 line priority encoder to obtain a three bit digital output equivalent of the applied analog input.




| Thermometer code | | | | | | | Binary code | | |
|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | B1 | B2 | B3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Fig.6. Conventional Flash ADC and truth table of priority encoder.

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The possible outputs of the comparators are tabulated. The truth table of priority encoder is as shown in Fig. 6 [5]. The binary code of the corresponding comparator output is obtained from the truth table.

## 4. Proposed Flash ADC

To reduce the number of comparators in flash ADC design multi-input comparators are used. To design n-bit flash ADC, only 'n' number of comparators are required. 3-bit Flash ADC is designed using multi-input comparator as shown in Fig.7. The Flash ADC design is simulated in 180-nm CMOS technology and the output is shown in Fig. 8.

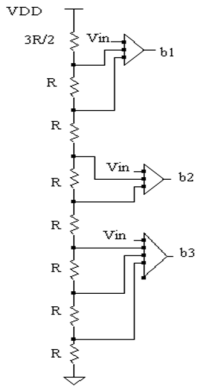


Fig. 7 Flash ADC with Multi-input Comparator.

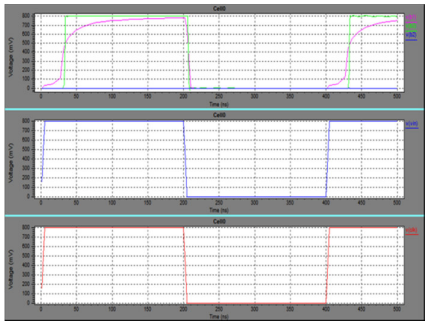

Fig. 8 Flash ADC output.

## 5. Simulation Results

Simulations are carried out in 180-nm CMOS technology using Tanner EDA tool. The performance of the conventional dynamic, double-tail, improved double-tail, conventional 3-bit flash ADC and proposed 3-bit flash ADC is tabulated as shown. Comparing the delay and power consumption it is evident that improved double-tail comparator can be used to design the conventional flash ADC.

Multi-input comparator is used to design the proposed Flash ADC. The total node count and power consumption is reduced in the proposed design.

Table I.1 Performance Results

| Design | Power consumption (watts) | Total node count | Delay (µs) |
|---|---|---|---|
| Conventional dynamic comparator. | $7.04 \times 10^{-6}$ | 11 | 47 |
| conventional double-tail comparator | $1.5 \times 10^{-5}$ | 14 | 10 |
| Improved double-tail comparator | $1.3 \times 10^{-5}$ | 18 | 7 |
| Conventional Flash ADC | $1.063137 \times 10^{-4}$ | 96 | 65 |
| Proposed Flash ADC | $9.711002 \times 10^{-5}$ | 51 | 42 |

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## 6. Conclusion

Improved double-tail comparator design produces reduced power and delay, compared to the conventional double-tail design. Conventional 3-bit flash ADC is designed using improved double-tail comparator. The number of comparison stages of the comparator is further increased, so that more inputs can be compared within a single clock cycle. Thus reduced area and power efficient Flash ADC design is obtained using the multi-input comparator.

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