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Design and Implementation of Down Sampler Using Multirate Technique

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Abstract- *A low power high speed VLSI design methodology based on multirate approach is presented in this paper. For a various input and output sampling rate multirate techniques are widely used as recent multirate device is down sampler. Filtering is adopted for multirate modules in order to provide signal processing in wireless communication. FPGA implementation is presented in this device whose results are verified and report is presented.*

In order to build up the sampler in require shift register D F/F and multiplexer are downloaded on cyclone II FPGA of ALTRA QUARTUS II. Designing all includes MCM and digital serial adder which reduce a complexity design in which digital circuit architecture is independent of data word length and required less area. The process of MCM is to reduce addition and subtraction in polyphase filter .The main objective of low power VLSI is to reduce hardware complexity and increases the speed.

INTRODUCTION

Multirate system got popularized in early 1980's which is commonly used in audio and video processing .The main objective of the multirate technique is to reduce the computational complexity. In essential signal processing component multirate filters is one among them where Finite Impulse Response (FIR) filters used to reduce the group delay. It is used when more than one sample rate is needed. Power delay products in VLSI are most essential metric of performance. This methodology provides technical way to derive the circuit at high speed and low voltage. Hence low power VLSI is systematically design to reduce the total power consumption. The down sampler used here is one of the reasons to reduce the sample rate. The number of addition and subtraction in polyphase filter is reduced by Multiple Constant Multiplication. In digital signal processing FIR filters is advantageous because it provide exact linear phase.

In this paper we propose resourceful low power FIR filter architecture, scheduled on the amplitude of filter coefficient and input the order of the filter can be vigorously changed. In the previous effort focused on reducing power consumption by maintaining a fixed filter order. Based on these approach the structure of FIR filter is simplified to add and shift operation and also by reducing the addition/subtraction. The main drawbacks of the previous approach are once the filter architecture is decided the coefficient cannot be changed.

Literature Survey

In this we will discuss about the various types of parameters and study about the research work of different authors ,how they make use of the filters ,adders and many other parameters to answer the problems and what are their future works .still now there are so many contributions which try to improve power efficiency Shahnam Mirzaei ,Anup Hosangadi, Ryan Kastner these author has

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proposed the performance of high speed Finite Impulse Response (FIR) filter just by using register adder and hardwired shift. The main objective is to reduce the adder here the software used is Xilinx Virtex II device in which implementation is compare with those produced by Xilinx coregenTM. The main advantage of this methodology is 50% in active power consumption. The author suggested that in future they would like to alter the algorithm to reduce the number of multipliers on FPGA device

Yun-Nan Chang, Janardhan H.Satyanarayana, Keshab K.Parhi the proposed method of this author is by increase the sample speed by reducing the power supply. This methodology can be pipelined at bit level and resultant power can be reduced. The tool used here is HEAT in which 35% of the power is obtained. The power consumed here is by bit-serial design due to high speed clock. The author says that in future the low power digital-serial multiplier will be designed with saturation capability

Bahram Rashidi, Farshad Mirzaei, Majit Pourormazd the proposal of this author is by implementing low power and low area digital Finite Impulse Response (FIR) filter. This method is for reducing dynamic power consumption of FIR filter used on low power multiplexer based on shift/ add multiplier without clock pulse. The minimum power achieved 56 Mw in FIR filter based on shift/add multiplier in 100 MHZ with 8 bits input and 8 bits coefficient. The tools used are Xilinx ISE V7.1 and virtex IV FPGA. The power is analyzed using Xilinx X power analyzer

Ranjendran N .Rewatkar, Dr.Sanjay L.Badjate the proposal of this author is systematic VLSI design of low power and area by means of multirate digital signal processing system. Since multirate is used different input and output sampling rate is required. The software for implementation used here is Cyclone II FPGA of ALTERA QUARTUS II platform. The data rate present in the multirate execution is M-times slower than the original data. The multirate implementation provides direct and efficient way to compensate the speed in low power design. In future the author effort will be directed towards transistor level implementation with full custom design and optimization level to obtain very low power and area and high speed.

Richa Maheshwari, Manisha Bharadia, and Meenakshi Gupta here they discussed about two basic operations in multirate system that is decimators and interpolator which increases and decreases the sampling rate of the signal. The sampled data result in the cast reduction of analog signal. Here the signal quality is improved by converting a sampling data signal to analog signal by combination of DAC and analog low-pass filter increasing in sampling rate result in distortion.

Proposed Work

In this proposed work multirate technique is used with various input and output sampling rate. Multirate module used for filtering to provide signal processing in wireless communication system. MCM and digital serial adder helps in reduction of low complexity design. In VLSI system power consumption is an important process and it is also one of the critical design parameters. The design of interpolation and decimation is implemented and the term power consumption area and the speed is determined.

Methodology

The methodology of this work is based on three phases

- Top level full custom design which is transistorize multirate module is developed with voltage and technological scaling
- Area, power and speed efficiency using MCM-digit architecture used for improving the parameters and reduce the complexity
- Interpolator and decimator is efficiently used and is applicable in wireless communication

Experimental Analysis

Transisterized Module of Down Sampler

Using Xilinx software transistorized module of downsampler is designed and parameter is analized. AMI 0.6 micro m and TSMC 0.25 micro m which helps in improving the parameter

Table1-Transistorized module of downsampler

Tech	AMI 0.6 µm		TSMC 0.35 µm		TSMC 0.25 µm	
V	Speed GHz	Power nW	Speed GHz	Power nW	Speed GHz	Power nW
1v	0.2337	0.1404	1.9093	0.64	0.8267	0.27
2v	0.4882	0.0673	1.1972	0.099	2.7716	0.063

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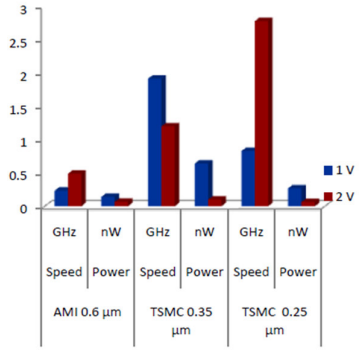

Phase-II: Multirate FIR Filter Design

To improve the parameters and to avoid circuit complexity Multirate FIR filter is designed. Power and area in system is reduced at great extend as multiplier, adders and latches are reduced by minimized by logic. In existing design constant multiplier block uses shift-add techniques. Shift unit will not use any area hence total cell area is reduced. In previous design 32 full adders are used but it requires only two adders. It is efficient technique in which compact power utilization and area by large value maintaining at higher speed.

Table2

Filter Name	Total cell Area(μm^2)	Total Dynamic Power	Speed
FIR Filter 0	28454.59761	5.8277 mW	32.624MHz
FIR Filter 1	34626.36188	12.7854 mW	-
FIR Filter 2	20999.76688	2.3450 mW	194.666MHz
FIR Filter- digit serial adder	28836.13853	5.8902 mW	-
Using MCM-digit serial adder	13424.32676	7.3128 mW	-
MCM- digit serial adder–shift adds	**988.815092**	**0.14922 mW**	**153.794MHz**

Conclusion

The reason technology is to improve the parameter using multirate techniques. The essential parameter is improved by AIM 0.6 micro m, TSMC 0.35 micro m and TSMC 0.35. This techniques improves the speed and power dissipation. Decimator and Interpolator are newly developed. MCM digital-serial design is given great attention which provide low complexity in operation. The results are verified using FPGA. This techniques can be implemented in applications such as antennas, speech, audio and video processing.

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